



# MCS-40™ PROTOTYPE SYSTEM

MCS-40 SYSTEM B

## MCS-40 SYSTEM — INTEL'S LOWEST COST MICROCOMPUTER. IDEAL FOR PROTOTYPE OR LOW VOLUME PRODUCTION AND RANDOM LOGIC REPLACEMENT.

The MCS-40 Microcomputer gives the user the design and computational capability of larger and more complex computers with just a small assortment of easy to use components. The set of parts are designed to offer the user an economical alternative to random logic.

The basic kit consists of the following standard building blocks:

- 4040 CPU
- 4269 Programmable Keyboard/Display Device
- 4265 Programmable General Purpose I/O
- 2111A 256 x 4 Static RAM
- 4289 Standard Memory Interface with I/O
- 4702A Programmable ROM
- 4201A System Clock

Due to the high degree of modularity of the MCS-40 system, additional components can be added to the kit to optimize it for the user's unique application. All components are fabricated with silicon gate, low threshold, PMOS technology.

The MCS-40 systems interface easily with switches, keyboards, displays, printers, communication terminals, and other popular peripherals. The 4269 Programmable Keyboard/Display greatly facilitates keyboard and display interfaces because of its automatic hardware support of functions such as keyboard scan and display refresh. The 4265 Programmable General Purpose I/O device allows easy interfacing to synchronous and asynchronous I/O devices, 8-bit peripheral devices, 8-bit microcomputers and standard memory devices such as the 2111A RAM.

A system built with the MCS-40 microcomputer set can have up to 8K x 8 of program memory in ROM or PROM, 1280 x 4-bit of RAM data memory and over 128 I/O lines, without requiring any interface logic. Further expansion of this very powerful system is accomplished with the addition of a few simple gates.

The MCS-40 Microcomputer has a very extensive instruction set which designers find extremely easy to use. The instruction set includes 60 powerful instructions, including true interrupt and a single step mode of operation. The basic instruction set consists of:

- Binary and Decimal Arithmetic
- Logical AND and OR
- Add and Subtract from Memory
- Rotate, Complement, and Test Accumulator
- Increment Registers
- Exchange Registers with Accumulator
- Conditional and Unconditional Branches and Subroutine Calls
- Increment, Test, and Branch in Single Instructions
- I/O Instructions
- Special Keyboard Instruction
- Interrupt Enable/Disable
- ROM and Register Bank Switching

In addition to the large assortment of MCS-40 components, Intel offers a complete line of resident and cross software products, hardware development aids such as the Intellec® 4/MOD 40 development system, user field training courses and an extensive staff of field application engineers to assist you with your unique design.

### Programmable General Purpose Microcomputer

**Program Storage in 4702A Reprogrammable PROM Simulates ROM**

**Instructions (60 total) including Logical Operations and Read Program Memory**

**Large Number of Family Devices**

**10.8 Microsecond Instruction Cycle Standard**

**Interrupt Capability**

**Single Step Operation**

**8K Byte Memory Addressing Capability**

**24 Index Registers**

**Subroutine Nesting to 7 Levels**

**2-Phase Dynamic Operation**

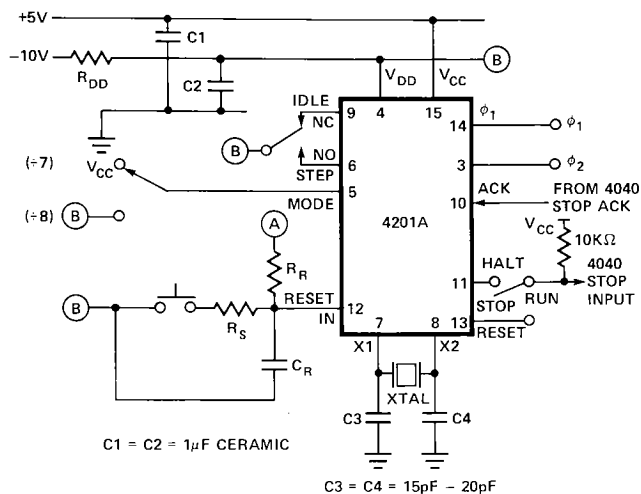
**Instruction Set Includes Conditional Branching, Jump to Subroutine and Indirect Fetching**

**Logical Instructions**

**Binary and Decimal Arithmetic Modes**

**Unlimited Number of Input and Output Lines**

## 4201A Implementation



## Design Considerations

### CRYSTALS

Either ÷7 or ÷8 Modes may be used. Mode equals  $V_{CC}$  for ÷7, Mode equals  $V_{DD}$  for ÷8. The clock frequency range should be between 500 kHz (4 MHz XTAL, ÷8 MODE) and 740 kHz (5.185 MHz XTAL, ÷7 MODE). The crystal may be found as a standard product from Intel distributors, CTS Knights or Crystek.

### X1 AND X2 INPUT CAPACITANCE

The XTAL terminals, X1 and X2, should be tied to 15 pF - 20 pF capacitors C3 and C4 to AC system GND.

### POWER SUPPLY VOLTAGE CONSIDERATIONS

- Operation is guaranteed with  $V_{CC}-V_{DD} = 15V \pm 5\%$ . During system power-up or during power supply glitching, the maximum magnitude of  $(V_{CC}-V_{DD})$  must be limited to 17 volts.

During the power supply rise time (that is, when  $|V_{CC}-V_{DD}| < 14.25$  volts), improper  $\phi_1$  and  $\phi_2$  output may occur until  $|V_{CC}-V_{DD}|$  reaches the 14.25 minimum voltage.

- With  $V_{CC} = +5V$ ,  $V_{DD} = -10V$ , bypass capacitor C1 of 1  $\mu F$  and C2 and 1  $\mu F$  in parallel from  $V_{CC}$  to GND and  $V_{DD}$  to GND, respectively, should provide excellent bypassing. Bypass capacitors should be ceramic or equivalent quality to insure low inductance and low series resistance.
- The purpose of the current limiting resistor  $R_{DD}$  is both to limit  $\phi_1$  and  $\phi_2$  rise times and to drop  $V_{DD}$  at the 4201A  $V_{DD}$  pin. Values for  $R_{DD}$  as a function of  $\phi_1$ ,  $\phi_2$  load capacitance are:  
For  $C_{LOAD} < 50$  pF; use  $R_{DD} = 100\Omega$ .  
For  $50$  pF  $< C_{LOAD} < 100$  pF; use  $R_{DD} = 68\Omega$ .  
For  $100$  pF  $< C_{LOAD} < 300$  pF; use  $R_{DD} = 27\Omega$ .  
For  $C_{LOAD} > 300$  pF; use  $R_{DD} = 10\Omega$ .

All 4201A functions requiring the  $V_{DD}$  voltage should use the pin  $V_{DD}$  or node (B) on the 4201A side of resistor  $R_{DD}$ . Operation with the voltage drop across  $R_{DD}$  is guaranteed by Intel testing.

### 4. Single-Supply System (+15 V or -15)

Recommended 4201A circuit modifications for single supply systems are:

- The 1  $\mu F$  ceramic capacitor C1 should be between 4201A  $V_{DD}$  and  $V_{CC}$  pins.
- Other capacitors shown as being grounded should be connected to  $V_{CC}$ .
- Reset  $R_R$  is connected to  $V_{CC}$ . Reset  $C_R$  is connected to  $V_{DD}$  pin.
- The current limiting resistor  $R_{DD}$  is still needed. in the  $V_{DD}$  line.

### 5. Power Supply Rise Times

Intel testing is for power supply rise times between 5 ms and 300 ms. For power supply rise times less than 5 ms, a 200K $\Omega$  resistor from X1 to GND and  $C3 = C4 = 5$  pF is recommended.

### RESET NETWORK

The Reset input has  $V_{IL} = V_{CC} - 11$  volts and  $V_{IH} = V_{CC} - 6.5$  volts, with about 1 volt of hysteresis (Schmitt circuit).

Node (A) must be tied to GND or  $V_{CC} = +5V$ ; and  $R_R$  and  $C_R$  selected, such that the negative  $V_{DD}$  transition moves the Reset input below  $V_{IL}$ .

Tying node (A) to GND and making  $C_R$  very large, i.e.  $> 1\mu F$ , will allow the greatest freedom in  $V_{CC}$  and  $V_{DD}$  rise times during turn-on. Tying node (A) to GND will also cause Reset after a  $V_{DD}$  glitch to GND.

The purpose of  $R_S$  at 510 $\Omega$  or 1K $\Omega$  is to limit Reset input fall time on manual Reset, so that the Reset input does not fall below  $V_{DD}$ .

### TTL CLOCK OUTPUTS

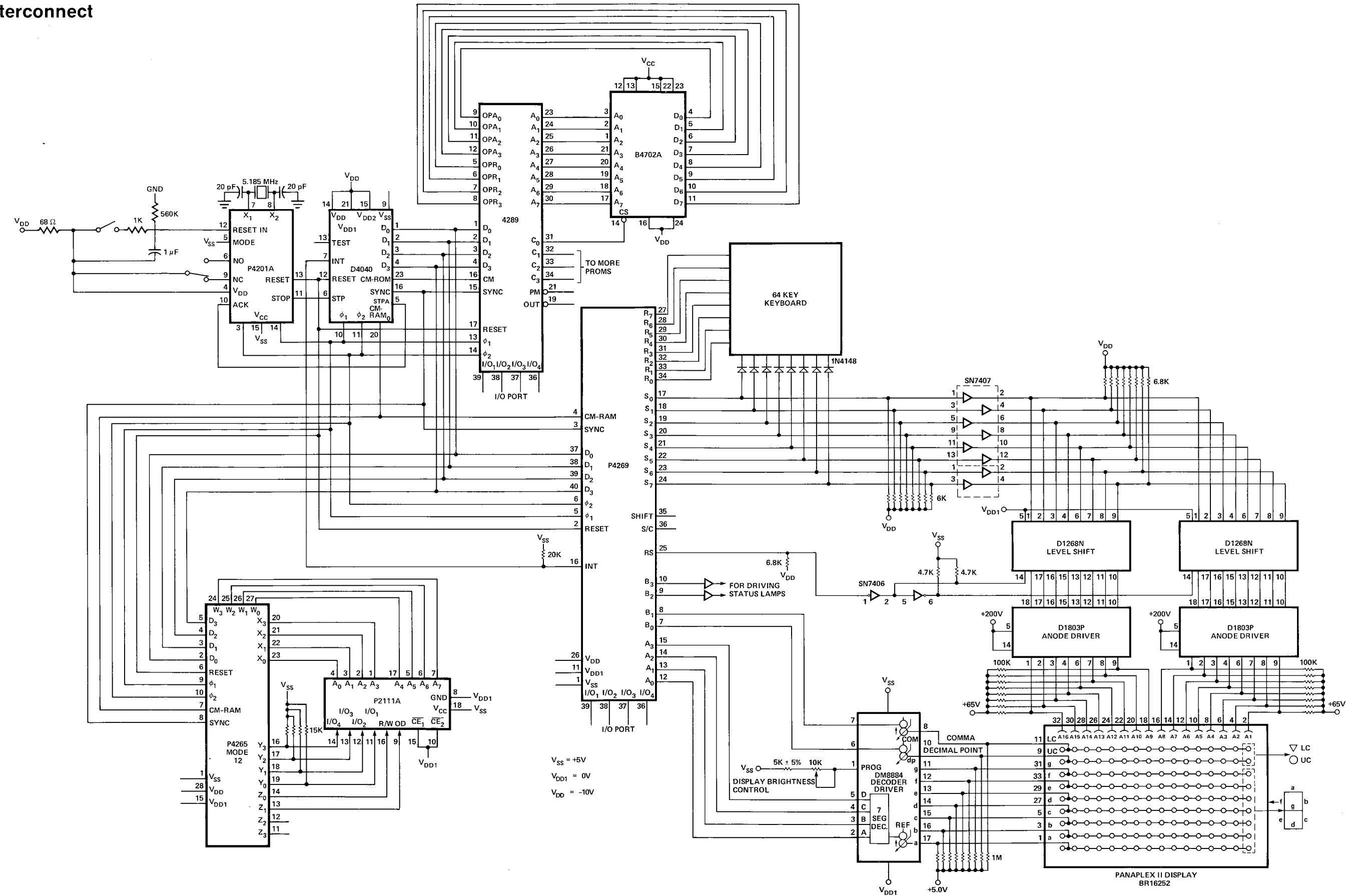
If  $\phi_{1T}$  and  $\phi_{2T}$  are used, GND pin should be tied to logic ground.  $\phi_{2T}$  levels will swing between  $V_{CC}$  and GND.

### UNUSED FUNCTIONS

If any of the 4201A functions listed below are not used, for power conservation it is recommended that the pins be connected as described below:

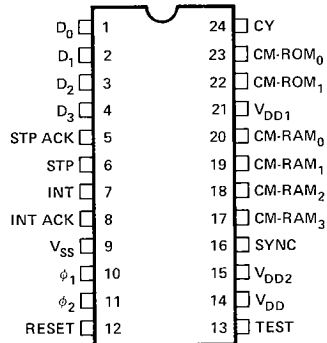
- $\phi_{1T}, \phi_{2T}$   
Tie GND pin,  $\phi_{1T}, \phi_{2T}$  to  $V_{CC}$ .
- Single step  
Tie NO to  $V_{CC}$ .  
Tie NC to Node (B) ( $V_{DD}$  pin).  
Tie STOP ACK to  $V_{CC}$ .  
STOP left open.
- Reset  
Tie RESET IN, RESET OUT to  $V_{CC}$ .

System Interconnect

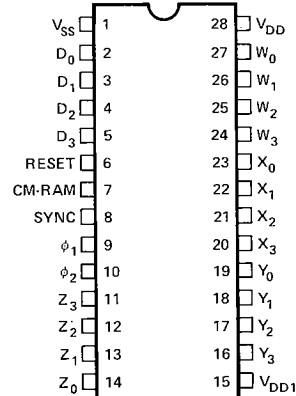


## Pin Configurations

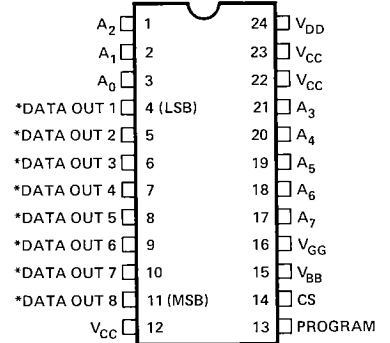
4040 CPU



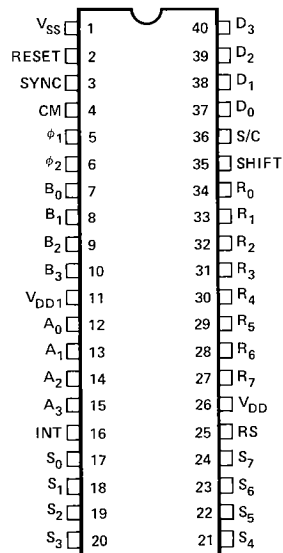
4265 GP I/O



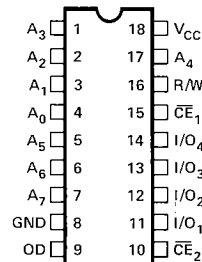
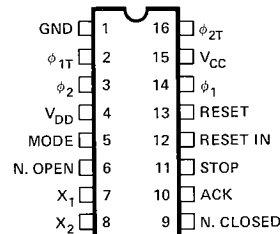
4702A ROM



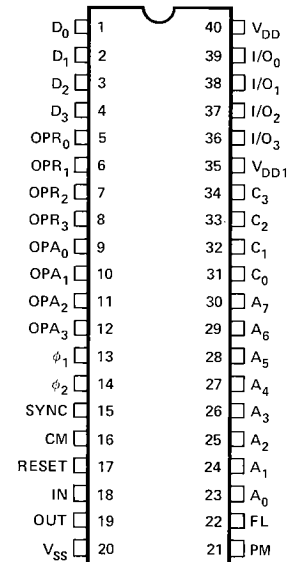
\*THIS PIN IS THE DATA INPUT LEAD DURING PROGRAMMING

4269  
KEYBOARD/DISPLAY

2111A RAM

4201A CLOCK  
GENERATOR

4289 INTERFACE





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